AMENDMENTS TO THE CLAIMS

REQUESTED MC

1. A method of reducing electrical power consumption by a digital computer when said digital computer is supplied with electrical power, but fails to process a computer application program for a prescribed period of inactivity, said digital computer including a host processor, said method comprising the computer implemented steps of:

said host processor producing and maintaining an internal context, said host processor containing code morphing software for dynamically translating and executing target applications designed for execution by a target processor, whereby said host processor creates a virtual target processor, said host processor maintaining data representing the state of said virtual target processor during processing of instructions of a target application and said internal context of said virtual target processor, said digital computer also including a private memory for storing at least the state of said virtual target processor and target application and said internal context of said virtual target processor;

determining if said prescribed period of inactivity has been attained, and, in response to an affirmative determination;

preserving said internal context of said virtual target processor against loss due to removal of electrical power from said host processor, said internal context of said

virtual target processor preserved in said private memory, wherein said private memory is accessible only by said host processor and powered independently of said host processor;

producing a signature in response to said determining to indicate that said private memory contains information;

removing all electrical power from said host processor, whereby said host processor is powered down, notwithstanding continued supply of electrical power to said digital computer; and

restoring electrical power to said host processor and restoring said preserved internal context of said virtual target processor to said host processor when processing is to resume.

2. The method defined in claim 1, wherein said step of preserving said internal context of said virtual target processor against loss due to removal of electrical power from said host processor, includes:

reading said internal context of said virtual target processor from the internal memory of said host processor prior to removal of electrical power from said host processor, said internal memory comprising internal registers; and

writing said internal context of said virtual target processor into said private memory.

REQUESTED MC

3. The method as defined in claim 1 wherein said host processor includes a cache memory; and wherein said step of preserving said internal context of said virtual target processor, includes:

supplying electrical power to said cache memory separately from said host processor, wherein removal of electrical power from said host processor leaves electrical power to said cache memory unaffected to prevent loss of said internal context of said host processor on removal of electrical power from said host processor.

4. The method as defined in claim 1, wherein the step of restoring electrical power to said host processor and restoring said preserved internal context of said virtual target processor to said host processor when processing is to resume, further comprises:

initializing said host processor;

determining whether application of electrical power was due to a power on reset condition or a resume from a suspend to RAM condition; and

upon determining that electrical power commenced due to a resume from a suspend to RAM condition, then accessing and installing said preserved internal context of said virtual target processor to said host processor.

REQUESTED MC

5. The method as defined in claim 1, wherein said step of restoring electrical power to said host processor and restoring said preserved internal context of said virtual target processor to said host processor when processing is to resume, further comprises:

initializing said host processor;

determining whether restoration of electrical power to said host processor is due to a power on reset condition or a resume from a suspend to RAM condition; and

upon determining that electrical power commenced due to a resume from a suspend to RAM condition, then accessing said preserved internal context of said virtual target processor in said private memory and reading back said internal context of said virtual target processor into internal registers of said host processor for access by said host processor, whereby said internal context of said virtual target processor of said host processor is restored.

6. (Canceled).

7. A processing system, comprising:

a central processing unit (CPU) for processing instructions of an application, said central processing unit including internal registers;

a first memory;

a second memory accessible only to said CPU;

REQUESTED MC

a power supply for supplying power separately to said CPU and said first and second memories, wherein said CPU, said first memory and said second memory each reside in separate power domains;

said power supply including:

a rechargeable battery;

first power circuit means for distributing electrical power to said CPU;

second power circuit means for distributing electrical power to at least said first memory and said second memory; and

an on-off switch for closing power from said battery to each of said first and second power circuit means, whereby said first and second power circuit means are enabled to deliver power;

first program routine means for detecting inactivity of application instruction processing of said CPU for a period of time, Tmax;

second program routine means for saving the internal context of said CPU in said second memory and for producing a signature in response to a positive detection of inactivity by said first program routine means, said signature indicating that said second memory contains information;

third program routine means for terminating distribution of power by said first power circuit means

following completion of said second program routine means, whereby power is removed from said CPU while said internal context of said CPU is preserved in said second memory.

8. The processor as defined in claim 7, further comprising:

a user operated input device for enabling user input to said application;

means for enabling said second power circuit means to distribute power to said CPU, responsive to operation of said user operated input device;

program means responsive to re-energization of said CPU for initiating an initialization process for said CPU;

loading and processing a boot loader;

configuring internal memory of said CPU, excluding said second memory;

resetting registers of said CPU; and

checking for said signature;

fourth routine program means, responsive to detection of said signature, for retrieving the portion of said internal context of said CPU earlier stored in said internal memory of said CPU and reading back said portion of said internal context of said CPU into the internal registers of said CPU, and retrieving said context of said Northbridge registers and loading said context of said Northbridge registers in said internal memory of said CPU.

REQUESTED MC

9. The processor as define in claim 8, further comprising:

fifth routine program means for retrieving the next instruction of the application program for execution by said CPU, responsive to completion of said fourth routine program means.

10. A processing system, comprising:

a central processing unit for processing instructions, said central processing unit including internal registers;

a first memory;

a second memory accessible only to said central processing unit;

code morphing program means defining a virtual X86 processing system, said virtual X86 processing system including a virtual X86 central processing unit and a virtual Northbridge chip, whereby instructions of an X86 application may be processed in said processing system;

a power supply for supplying power separately to said CPU and said first and second memories, wherein said CPU, said first memory and said second memory each reside in separate power domains;

said power supply including:

a rechargeable battery;

REQUESTED ML

first power circuit means for distributing electrical power to said CPU;

second power circuit means for distributing electrical power to at least said first and second memory; and

an on-off switch for closing power from said battery to each of said first and second power circuit means, whereby said first and second power circuit means are enabled to deliver power;

first program routine means for detecting inactivity of application instruction processing of said CPU for a period of Tmax;

second program routine means for saving the entire internal context of said CPU in said second memory and for producing a signature in response to a positive detection of inactivity by said first program routine means, said signature indicating that said second memory contains information;

third program routine means for terminating distribution of power by said first power circuit means following completion of said second program routine means, whereby power is removed from said CPU and said CPU is placed in an off state while said internal context of said CPU is preserved in said second memory.

11. The processor as defined in claim 10, further comprising:

REQUESTED mc

means for enabling said second power circuit means to distribute power to said CPU, responsive to operation of said user operated input device;

program means responsive to re-energization of said CPU for initiating an initialization process for said CPU;

loading and processing a boot loader;

configuring internal memory of said CPU, excluding said second memory;

resetting the registers of said CPU; and

checking for said signature;

fourth program routine means, responsive to detection of said signature, for retrieving the portion of said internal context of said CPU earlier stored in one of said first and second memory and reading back said portion into the internal registers of said CPU, and retrieving said context of said Northbridge registers earlier stored in one of said first and second memory and loading said context in said internal registers of said CPU.

12. A digital computer comprising: a CPU; a private memory accessible only by said CPU; and a power supply, said power supply for supplying power to said CPU and said private memory independent of one another to enable withdrawal of power from said CPU without withdrawal of power from said private memory; said CPU defining and maintaining a CPU context to enable processing of

application programs; said CPU containing code morphing software for dynamically translating and executing target applications designed for execution by a target processor, whereby said CPU creates a virtual target processor, said CPU maintaining data representing the state of said virtual target processor during processing of instructions of a target application and said internal context of said virtual target processor; said private memory for storing at least the state of said virtual target processor and said target application, said internal context of said virtual target processor and said CPU context, whereby said CPU context is retained upon withdrawal of power from said CPU without withdrawal of power from said private memory and wherein a flag is set to indicate that said private memory contains said CPU context.

13. (Canceled).

14. A method of reducing power consumption of a digital computer during a sleep mode of operation, said digital computer including a power management program for placing said digital computer in multiple stages of sleep mode, said multiple stages of sleep comprising at least a pre-STR (suspend to RAM) stage and an STR stage, said method comprising:

determining whether a first instruction is issued by said power management program for placing said digital computer in a pre-STR stage of sleep, said pre-STR stage comprising maintaining power to a processor of said digital computer;

intercepting said first instruction; and

substituting for said first instruction a second instruction to place said digital computer in said STR stage of sleep, said STR stage comprising removing power from said processor, wherein entry to said STR stage occurs bypassing said pre-STR stage in response to said first instruction and transparent to said power management program.

15. The method of claim 14 further comprising:

writing internal context of said processor to a private memory accessible only by said processor and powered independently of said processor; and

removing power from said processor.

16. A computer system comprising:

a processor;

a first memory accessible by said processor;

a second memory accessible only to said processor, wherein said second memory is internal to said processor, wherein power to said second memory is controlled separately from power to said processor and to said first memory,

wherein power is maintained to said second memory when power is removed from said processor, said second memory for maintaining internal context of said processor when power is removed from said processor; and

a third memory external to said processor and accessible only to said processor, wherein power to said third memory is controlled separately from power to said processor and to said first and second memories.

Claims 17-19. (Canceled).